web extra

Panel Summary

Power-Aware Verification: Is It a Front-End or a Back-End Issue?

Thomas L. Anderson, Cadence Design Systems

Shankar Hemmady, Synopsys

Few topics are of more interest these days than low-power design. The plethora of battery-powered portable devices, rising energy costs, and "green" legislation are putting pressure on designers of nearly all electronic products to reduce power consumption. A wide range of techniques for managing and reducing power has emerged, many of which introduce significant complexity to the functional verification process. A panel at DesignCon 2009 in Santa Clara, California, addressed several key aspects of power-aware verification for low-power designs.

Panel chair Bhanu Kapoor, founder and president of Mimasic, set the stage by defining the "three Ps of design: price, performance, and power" thus reinforcing the critical importance of power for today's electronic devices. He said that power-management circuitry could be introduced at multiple points in the design flow, with different implications for how and where verification should occur. Kapoor challenged the panelists to address best practices for power-aware verification and how they can be automated to reduce effort and improve design quality.

Gary Delp, Distinguished Engineer from LSI, focused on using power specification files to guide logic-synthesis and place-and-route tools to insert power-management structures into the design automatically. He noted that the same files can enable verification tools to check that the inserted power logic works as expected and the functional operation of the design has not been compromised. He gave examples of power-aware verification at the front end, during simulation and formal analysis, and at the back end, during equivalence and electrical rule checking.

John Goodenough, director of design technology at ARM, described an advanced ARM media chip that has "tens" of different domains that can be turned off to save power. He talked specifically about experimenting with formal techniques on the power controller, a complex state machine sequencing the power-up and power-down of the different domains. He called for formal tool vendors to support verification that a power controller can make only the specific legal transitions documented in the power specification files.

Synopsys R&D Group Director Srikanth Jadcherla provided a daunting list of new classes of errors that can be introduced by low-power design. These include isolation and level-shifting bugs, illegal power controller transitions, errors in saving and restoring state for powered-down domains, and deadlocks. He also pointed out that some chips are designed such that turning on all domains at full power will trigger thermal runaway and device destruction. A rigorous verification methodology ensures that the chip can never get into a runaway state and that bugs don't escape.

The final panelist was Shireesh Verma, senior staff engineer at Conexant, presenting an "engineer's perspective" on low-power design and verification. He reinforced the importance of checks for proper power gating, isolation, and state retention. He expressed some dismay over the "steep learning curve" associated with some power-aware commercial EDA tools. He said that he has used mostly internally developed solutions but, since that takes a great deal of research and resources, he would prefer using commercial tools once they become more "palatable."

As with any timely panel topic, the audience asked provocative questions. The simplest question–how many power domains are in chips today?–turned out to have the longest answer. The consensus was that 2–5 domains are typical, with the average around 4. However, some panelists reported numerous designs with more than 20 power domains, including one chip with 86. Several panelists commented that the number of unique legal power modes (on-off combinations) is more relevant for verification than the number of power domains.

The panelists concluded that power-aware verification necessarily entails tools and methodology that span both the front and back ends of the flow. There was a clear consensus that the availability of a power specification file is a key enabler for this process, and that the specific format of this file is unimportant as long as it can accurately express power intent. Given such a file, most power management structures can be created automatically, and most of the low-power functionality can be verified automatically by commercial EDA tools.

DesignCon 2010, including its IP and PCB Summits, will take place in Santa Clara, California, 1–4 Feb. 2010 (http://www.designcon.com/2010/).

This Web extra accompanies the article, "Conference Reports and Panel Summaries," IEEE Design & Test of Computers, vol. 26, no. 6, 2009, p. 95; http://doi.ieeecomputersociety.org/10.1109/MDT.2009.142.